

TITLE

PLASMA DISPLAY PANEL AND METHOD FOR DRIVING THE SAME

CLAIM OF PRIORITY

[0001] This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C. §119 from an application for "*PLASMA DISPLAY PANEL AND METHOD FOR DRIVING THE SAME*" earlier filed in the Korean Intellectual Property Office on 23 July 2002 and there duly assigned Serial No. 2002-43250.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a plasma display panel and a method for driving the same.

Description of the Related Art

[0003] A plasma display panel (PDP) is a type of display device that has a plurality of discharge tubes arranged in a matrix form, and it selectively makes them radiate to reconstitute picture data input as electrical signals. The driving method of the PDP is classified into a DC (direct current) driving method and an AC (alternating current) driving method, according to whether or not the polarity of the voltage applied to sustain a discharge is changed with an elapse of time.

[0004] The general PDP is a display device in which an ultraviolet ray emitted from a discharge of each pixel cell excites a fluorescent material coated on the inner wall of the pixel cell to realize

a desired color. To achieve color display, the PDP must exhibit an intermediate gradation. The method for exhibiting an intermediate gradation that is currently used involves dividing one TV field into a plurality of sub-fields and subjecting the sub-fields to time division control.

[0005] There are two methods for exhibiting an intermediate gradation: an ADS (Address Display Separated) driving method and an AWD (Address While Display) driving method.

[0006] As an example in the ADS driving method, in order to display a 256-gradation image, one frame is time-divided into eight sub-fields, each of which is subject to time division into a reset period to initialize a screen, an address period to sequentially scan the screen and write data, and a sustain discharge period to sustain the luminescent status of each data-written discharge cell for a predetermined period of time, thereby driving the PDP. Here, the address period is allocated equally to each sub-field, but the sustain discharge period is allocated to the respective sub-fields at a rate of 2^n (0, 1, 2, ..., 7). Then the respective sub-fields realize a gradation in proportion to the sustain discharge period, and the gradations of the respective sub-fields are combined into a gradation for an image of one frame.

[0007] The ADS driving method is problematic in that the brightness is too low, because the sustain discharge period is shorter than the address period. In addition, the sustain discharge must be activated again after addressing the whole screen, so that wall charges generated in the discharge cells are heterogeneous due to the elapsed time for the address period, thereby causing a false discharge and a heterogeneous discharge during the sustain discharge period and hence a deterioration of the image quality.

[0008] Unlike the ADS driving method, the AWD driving method does not involve time division

1 into a reset period, an address period, and a sustain discharge period. In the AWD driving method,
2 a sustain discharge pulse of a predetermined frequency is successively applied to scan and sustain
3 electrodes, and addressing is partly performed every period of the sustain discharge pulse. So the
4 sustain discharge occurs over one frame without a discontinuance. Advantageously, the AWD
5 driving method enhances the brightness because the sustain discharge period is sufficiently long.

6 **[0009]** In both the ADS driving method and the AWD driving method, however, the individual
7 sub-fields consist of a reset period, an address period, and a sustain discharge period, and a large
8 amount of ineffective light is generated due to reset and erase pulses in the reset period, resulting in
9 a deterioration of contrast.

10 SUMMARY OF THE INVENTION

11 **[0010]** It is therefore, an object to provide an improved apparatus and technique for driving a PDP.

12 **[0011]** It is another object to provide an apparatus and technique for driving a PDP with no more
13 than one reset pulse voltage being applied for one TV field without a reset step between the
14 respective sub-fields, thereby drastically reducing ineffective light and improving the contrast.

15 **[0012]** It is yet another object to provide an apparatus and technique for driving a PDP with a
16 plurality of scan and sustain electrodes being arranged so as to reduce the number of driver IC's for
17 the scan and sustain electrodes, thereby lowering the cost of the PDP.

18 **[0013]** In accordance with the present invention contrast is drastically improved by applying a
19 reset pulse voltage only once during one TV field while maintaining a high brightness.

20 **[0014]** In one aspect of the present invention, there is provided a method for driving a PDP which

includes a plurality of first and second electrodes arranged in pairs, a plurality of data electrodes formed normal to the first and second electrodes, and a plurality of sub-fields for one TV field to display a multi-gradation, the method including: (a) a reset step of applying a reset pulse voltage to the first electrodes; (b) a sustain discharge step of applying a first voltage alternately to the first electrodes and the second electrodes to cause a sustain discharge; and (c) an address erasure step of, after applying a second voltage to the first electrodes or removing part of the first voltage applied to the first electrodes, applying third and fourth voltages to the second electrodes and the data electrodes, respectively, before applying the first voltage, to erase wall charges in cells defined by the first electrodes, the data electrodes, and the second electrodes.

[0015] In another aspect, there is provided an apparatus for driving a PDP which includes a plurality of first and second electrodes arranged in pairs, a plurality of data electrodes formed normal to the first and second electrodes, and a plurality of sub-fields for one TV field to display a multi-gradation, the apparatus including: a first driver for applying a voltage for sustain discharge to the first electrodes by periods, and applying a first voltage to the first electrodes of cells selected for erasure of the sustain discharge or removing the voltage for sustain discharge to erase the sustain discharge; a second driver for applying the voltage for sustain discharge to the second electrodes, and applying a second voltage to the second electrodes of cells selected for erasure of the sustain discharge; and a third driver for applying a third voltage to the data electrodes of cells selected for erasure of the sustain discharge.

[0016] In still another aspect of the present invention, there is provided a PDP including: first and second substrates; a plurality of first and second electrodes arranged in pairs; a plurality of data

1 electrodes arranged alternately with the first electrodes and the second electrodes; a first driver for
2 applying a first voltage to the first electrodes by periods to cause a sustain discharge, and applying
3 a second voltage to the first electrodes of cells selected for erasure of the sustain discharge or
4 removing the first voltage to erase the sustain discharge; a second driver for applying a third voltage
5 to the second electrodes of cells selected for erasure of the sustain discharge before applying the first
6 voltage, after applying the second voltage to the first electrodes or removing the first voltage from
7 the first electrodes; and a third driver for applying a fourth voltage to the data electrodes of cells
8 selected for erasure of the sustain discharge before applying the first voltage, after applying the
9 second voltage to the first electrodes or removing the first voltage from the first electrodes.

10 [0017] Preferably, the plural first and second electrodes are divided into j groups each including
11 i pairs of the first and second electrodes, and the plasma display panel further includes j first
12 common lines and i second common lines, wherein the j first common lines are coupled
13 independently to the j groups, the first electrodes of the one group are coupled in common to the first
14 common line, and the i second electrodes of the same group are coupled independently to the i
15 second common lines.

16 BRIEF DESCRIPTION OF THE DRAWINGS

17 [0018] A more complete appreciation of the invention, and many of the attendant advantages
18 thereof, will be readily apparent as the same becomes better understood by reference to the following
19 detailed description when considered in conjunction with the accompanying drawings in which like
20 reference symbols indicate the same or similar components, wherein:

1 [0019] Fig. 1 is a schematic diagram of a PDP in accordance with an embodiment of the present
2 invention;

3 [0020] Fig. 2 is an electrode connection diagram of the PDP in accordance with an embodiment
4 of the present invention;

5 [0021] Fig. 3A is a waveform diagram of voltages applied to the common lines YY_1 , YY_2 , XX_1 ,
6 and XX_2 and the data electrode D_2 of Fig. 2;

7 [0022] Fig. 3B illustrates a discharge and a wall charge status in each cell at the respective time
8 points of Fig. 3A;

9 [0023] Fig. 4 is a driving waveform diagram showing the measurement of the margins of the scan
10 pulse voltage and the data pulse voltage of Fig. 3A;

11 [0024] Fig. 5 shows the absolute value $|V_{scan}|$ of the scan pulse voltage and the measurement of
12 the operational margin of the data pulse voltage V_{data} according to an embodiment of the present
13 invention;

14 [0025] Fig. 6 is a driving waveform diagram for measuring the operational margin of the scan
15 pulse voltage and the data pulse voltage according to an embodiment of the present invention;

16 [0026] Fig. 7 shows the maximum of the absolute value of the scan pulse voltage $|V_{scan}|$ according
17 to the change of T_{s-d} when the data pulse voltage is 0V, according to an embodiment of the present
18 invention;

19 [0027] Figs. 8 and 9 show the operational margin of the data pulse voltage for T_{s-d} when the
20 absolute value of the scan pulse voltage $|V_{scan}|$ is 70 V and 80 V, respectively, according to an
21 embodiment of the present invention;

1 **[0028]** Fig. 10 shows a driving voltage waveform of a PDP with a bias pulse voltage applied,
2 according to an embodiment of the present invention;

3 **[0029]** Fig. 11 shows the measurement of the operational margin of the data pulse voltage based
4 on the change of the bias pulse voltage according to an embodiment of the present invention;

5 **[0030]** Fig. 12 is a general electrode connection diagram of a PDP according to an embodiment
6 of the present invention;

7 **[0031]** Fig. 13 shows a driving voltage waveform for driving the PDP according to an embodiment
8 of the present invention; and

9 **[0032]** FIG. 14 shows an example of a computer including a computer-readable medium having
10 computer-executable instructions for performing a method of the present invention.

11 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

12 **[0033]** In the following detailed description, only the preferred embodiment of the invention has
13 been shown and described, simply by way of illustration of the best mode contemplated by the
14 inventor(s) of carrying out the invention. As will be realized, the invention is capable of modification
15 in various obvious respects, all without departing from the invention. Accordingly, the drawings and
16 description are to be regarded as illustrative in nature, and not restrictive.

17 **[0034]** Hereinafter, a description will be given as to a PDP according to an embodiment of the
18 present invention with reference to Figs. 1 and 2.

19 **[0035]** Fig. 1 is a schematic diagram of the PDP according to the embodiment of the present
20 invention.

[0036] The PDP according to the embodiment of the present invention includes, as shown in Fig. 1, a plasma panel 100, an address driver 200, a scan electrode (Y electrode) driver 320, a sustain electrode (X electrode) driver 340, and a controller 400.

[0037] The plasma panel 100 includes a plurality of data electrodes D_1 to D_m arranged in columns, and a plurality of scan and sustain electrodes Y_1 to Y_n and X_1 to X_n alternately arranged in rows.

[0038] The address driver 200 receives an address drive control signal S_a from the controller 400, and applies an address voltage for selection of a cell for erasure of sustain discharge to the corresponding data electrode.

[0039] The scan electrode driver 320 receives a scan electrode drive control signal S_y from the controller 400 and applies a sustain discharge voltage to the respective scan electrodes at predetermined intervals for sustain discharge, and a scan pulse voltage for selection of a cell selected to erase a sustain discharge to the corresponding scan electrode.

[0040] The sustain electrode driver 340 receives a sustain electrode drive control signal S_x from the controller 400, and applies a sustain discharge voltage to the respective sustain electrodes at predetermined intervals for sustain discharge. As will be described later, the sustain electrode driver 340 according to the embodiment of the present invention does not apply a sustain discharge voltage to the sustain electrode for a cell selected to erase a sustain discharge.

[0041] The controller 400 externally receives a picture signal to generate the address drive control signal S_a , the scan electrode drive control signal S_y , and the sustain electrode drive control signal S_x , and applies the control signals to the address driver 200, the scan electrode driver 320, and the sustain electrode driver 340, respectively.

[0042] Fig. 2 is an electrode connection diagram of the PDP according to an embodiment of the present invention. Expediently, the PDP as illustrated in the figure has four pairs of scan/sustain electrodes and three data electrodes.

[0043] In the figure, electrodes Y_1 to Y_4 , electrodes X_1 to X_4 , and electrodes D_1 , D_2 , and D_3 represent scan electrodes, sustain electrodes, and data electrodes, respectively. As shown in Fig. 2, the scan electrodes Y_1 to Y_4 and the sustain electrodes X_1 to X_4 are alternately arranged in rows, and the data electrodes D_1 , D_2 , and D_3 are arranged in columns.

[0044] In the PDP according to the embodiment of the present invention shown in Fig. 2, the electrodes are grouped in the units of four adjacent scan and sustain electrodes.

[0045] Namely, electrodes Y_1 , X_1 , Y_2 , and X_2 are included in a first group, and electrodes Y_3 , X_3 , Y_4 , and X_4 are included in a second group.

[0046] The first scan electrodes Y_1 and Y_3 of the first and second groups are coupled to a scan electrode common line YY_1 , and the second scan electrodes Y_2 and Y_4 of the first and second groups are coupled to a scan electrode common line YY_2 . Both the sustain electrodes X_1 and X_2 of the first group are coupled to a sustain electrode common line XX_1 , and both the sustain electrodes X_3 and X_4 of the second group are coupled to a sustain electrode common line XX_2 .

[0047] The PDP according to the embodiment of the present invention has scan and sustain driver ICs (integrated circuits), each of which is coupled to the common lines YY_1 , YY_2 , XX_1 , and XX_2 for driving the scan and sustain electrodes. Accordingly, the number of driver IC's is remarkably reduced in comparison with the conventional PDP that has sustain electrodes coupled in common and scan driver IC's coupled to every scan electrode.

[0048] Hereinafter, a description will be given as to a method for driving a PDP in accordance with an embodiment of the present invention with reference to Figs. 3A and 3B.

[0049] Fig. 3A is a waveform diagram of voltages applied to the common lines YY_1 , YY_2 , XX_1 , and XX_2 , and the data electrode D_2 , which explains the method for driving a PDP according to the embodiment of the present invention. Fig. 3B illustrates a discharge and a wall charge status in each cell at the respective time points of Fig. 3A.

[0050] Referring to Fig. 3A, before t_1 , a sustain discharge voltage (approximately 155 V) is applied alternately to the scan electrode common lines YY_1 and YY_2 , and the sustain electrode common lines XX_1 and XX_2 , to cause a sustain discharge in cells $Y_1-X_1-D_2$, $Y_2-X_2-D_2$, $Y_3-X_3-D_2$, and $Y_4-X_4-D_2$.

[0051] At t_1 , the sustain discharge voltage is applied to the scan electrode common lines YY_1 and YY_2 , and an electric potential of the sustain electrode common lines XX_1 and XX_2 is sustained at a ground voltage. As illustrated in Fig. 3B, a discharge occurs between the scan electrodes Y_1 , Y_2 , Y_3 , and Y_4 , and the sustain electrodes X_1 , X_2 , X_3 , and X_4 . Thus negative (-) wall charges are stored in the scan electrodes Y_1 , Y_2 , Y_3 , and Y_4 , and positive (+) wall charges are stored in the sustain electrodes X_1 , X_2 , X_3 , and X_4 . Priming particles are also generated in the discharge cells.

[0052] At t_2 , the scan electrode common lines YY_1 and YY_2 are sustained at a ground potential, and a sustain discharge voltage is applied to the sustain electrode common line XX_1 . But the sustain discharge voltage is not applied to the sustain electrode common line XX_2 , which is sustained at the ground potential.

[0053] In the cells $Y_1-X_1-D_2$ and $Y_2-X_2-D_2$, a discharge occurs between scan electrodes Y_1 and Y_2

and sustain electrodes X_1 and X_2 , as illustrated in Fig. 3B. Thus, positive (+) wall charges are stored in the scan electrodes Y_1 and Y_2 , and negative (-) wall charges are stored in the sustain electrodes X_1 and X_2 .

[0054] In the meantime, a discharge is not caused in the cells Y_3 - X_3 - D_2 and Y_4 - X_4 - D_2 , so that there remain negative (-) wall charges in the scan electrodes Y_3 and Y_4 and positive (-) wall charges in the sustain electrodes X_3 and X_4 .

[0055] At t_3 , a sustain pulse voltage (approximately -70 V) is applied to the scan electrode common line YY_1 , and a data pulse voltage (approximately 50 V) is applied to the data electrode D_2 , as illustrated in Fig. 3A. Then the wall charges of the cell Y_3 - X_3 - D_2 are all erased, as illustrated in Fig. 3B. With the wall charges erased, a discharge cannot be caused by an applied sustain discharge voltage. The wall charges in the other cells are sustained.

[0056] At t_4 , the ground voltage is applied to the scan electrode common lines YY_1 and YY_2 , and a sustain discharge voltage is applied to the sustain electrode common lines XX_1 and XX_2 . In the cells Y_1 - X_1 - D_2 and Y_2 - X_2 - D_2 , wall charges are generated: negative (-) wall charges in the scan electrodes Y_1 and Y_2 and positive (+) wall charges in the sustain electrodes X_1 and X_2 to cause a discharge, as illustrated in Fig. 3B. But a discharge does not occur in the cell Y_4 - X_4 - D_2 at t_4 , because there remain negative (-) wall charges in the scan electrode Y_4 and positive (+) wall charges in the sustain electrode X_4 .

[0057] In the cell Y_3 - X_3 - D_2 , no discharge occurs even with a sustain discharge voltage at t_4 , because wall charges in the cell are all erased at t_3 .

[0058] At t_5 , the ground voltage is applied to the scan electrode common lines YY_1 and YY_2 , and

a sustain discharge voltage is applied to the sustain electrode common lines XX_1 and XX_2 . Then a discharge occurs in every cell except for the cell Y_3 - X_3 - D_2 to generate positive (+) wall charges in the scan electrodes Y_1 , Y_2 , and Y_4 , and negative (-) wall charges in the sustain electrodes X_1 , X_2 , and X_4 , as illustrated in Fig. 3B. But no discharge occurs in the cell Y_3 - X_3 - D_2 , because wall charges in the cell are all erased at t_3 .

[0059] As described above, the method for driving a PDP according to the embodiment of the present invention uses a 3-input AND logic operation for selection of cells for erasure of the sustain discharge. Namely, the inputs of the 3-input AND logic operation include removing a sustain discharge voltage pulse, applying a scan pulse voltage to scan electrodes, and applying a data pulse voltage to data electrodes, thereby erasing a sustain discharge.

[0060] Hereinafter, a description will be given as to an operational margin of the driving voltage for the PDP according to the embodiment of the present invention, with reference to Figs. 4 and 5.

[0061] Fig. 4 is a driving waveform diagram for measuring margins of the scan pulse voltage and the data pulse voltage of Fig. 3A. T_{s-d} represents the time from the end of the sustain discharge to the start of the next scan pulse voltage application, which is $3\mu s$ (microseconds). All the scan and data pulses have a width of $0.33\mu s$.

[0062] Fig. 5 shows the absolute value $|V_{scan}|$ of the scan pulse voltage and the measurement of the operational margin of the data pulse voltage V_{data} according to the embodiment of the present invention. The voltage and the width of pulses used in the driving waveform diagram of Fig. 4 are presented in Table 1.

[0063] Table 1

	Pulse voltage	Pulse width (μs)
Sustain discharge pulse	155 V	2
Reset 1 pulse	-190V	2
Reset 2 pulse	145V	8
Scan pulse	V_{scan}	0.33
Data pulse	V_{data}	0.33

[0064] In Fig. 4, an address erasure occurs even when the cell Y_3 - X_3 - D_2 defined by the scan electrode common line YY_1 , the sustain electrode common line XX_2 , and the data electrode D_2 are selected (refer to Fig. 2). If the absolute value of the scan pulse voltage $|V_{scan}|$ exceeds 82 V in this case, a discharge occurs without a data pulse voltage being applied. Alternatively, if the data pulse voltage V_{data} exceeds 76 V (volts), a discharge occurs without a scan pulse voltage being applied. For the address erasure, the sum $|V_{scan}| + V_{data}$ of the absolute value of the scan pulse voltage and the data pulse voltage must exceed 90 V.

[0065] For unselected cells, a unnecessary discharge occurs between the data electrode and the sustain electrode when the data pulse voltage V_{data} exceeds 60 V, and between the data electrode and the scan electrode when the sum $|V_{scan}| + V_{data}$ of the absolute value of the scan pulse voltage and the data pulse voltage exceeds 210 V.

[0066] Accordingly, the operational margin of the data pulse voltage and the scan pulse voltage according to the embodiment of the present invention is the overlapping area (defined by lines A, C, and E) of the operational margin area of the selected cell (defined by lines A, B, and C) and the

operational margin area of the unselected cells (defined by lines D and E).

[0067] Hereinafter, a description will be given as to the operational margin of the scan pulse voltage and the data pulse voltage when the time T_{s-d} from the end of the sustain discharge to the start of the next scan pulse voltage application is variable between $2.33\ \mu s$ and $7.33\ \mu s$, with reference to Figs. 6 to 9.

[0068] Fig. 6 shows a driving waveform for measuring the operational margin of the scan pulse voltage and the data pulse voltage according to the embodiment of the present invention. The driving waveform of Fig. 6 is the same as that of Fig. 4, excepting that T_{s-d} is variable between $2.33\ \mu s$ and $7.33\ \mu s$,

[0069] Fig. 7 shows the maximum of the absolute value of the scan pulse voltage $|V_{scan}|$ according to the change of T_{s-d} when the data pulse voltage is 0V, according to the embodiment of the present invention.

[0070] In Fig. 7, the maximum of the absolute value of the scan pulse voltage $|V_{scan}|$ increases with an increase in T_{s-d} , because the priming effect caused by the sustain discharge is reduced with the greater T_{s-d} .

[0071] As can be seen from Fig. 7, T_{s-d} must be longer than $2.33\ \mu s$ for $|V_{scan}|$ of 70V and $2.8\ \mu s$ for $|V_{scan}|$ of 80 V. Because the data pulse width is $0.33\ \mu s$, 16 data pulses can be applied during a time period of 0.33 to $7.33\ \mu s$ when $|V_{scan}|$ is 70 V; and 14 data pulses can be applied during a time period of 2.8 to $7.33\ \mu s$ when $|V_{scan}|$ is 80 V.

[0072] Figs. 8 and 9 show the operational margin of the data pulse voltage for T_{s-d} when $|V_{scan}|$ is 70 V and 80 V, respectively, according to the embodiment of the present invention. An address

1 erasure occurs adequately when the data pulse voltage V_{data} exceeds the minimum data pulse voltage
2 value. But an unnecessary discharge occurs when the data pulse voltage V_{data} exceeds the maximum
3 data pulse voltage value. The minimum and maximum data pulse voltage values increase with an
4 increase in T_{s-d} , because the number of priming particles is reduced.

5 **[0073]** In Figs. 8 and 9, T_{s-d} is variable between 3 and 7.33 μs . For $|V_{scan}|$ of 70 V, the margin of
6 the data pulse voltage is 14 V as defined by the area between the dotted lines in Fig. 8. For $|V_{scan}|$
7 of 80 V, and the margin of the data pulse voltage is 25 V as defined by the area between the dotted
8 lines in Fig. 9.

9 **[0074]** But, when the scan and data pulses having a width of 0.33 μs are applied in succession,
10 these pulses are combined to broaden the pulse width. With an increase in the pulse width, the
11 minimum data pulse voltage increases and thereby the operational margin of the data pulse voltage
12 decreases.

13 **[0075]** To compensate for the reduced operational margin of the data pulse voltage with the
14 broadened pulse width, a bias pulse voltage is applied between the sustain discharge pulses.
15 Hereinafter, a description will be given as to the operational margin of the data pulse voltage based
16 on the bias pulse voltage applied, with reference to Figs. 10 and 11.

17 **[0076]** Fig. 10 shows a driving voltage waveform of a PDP with a bias pulse voltage applied,
18 according to the embodiment of the present invention, and Fig. 11 shows the operational margin of
19 the data pulse voltage based on the change of the bias pulse voltage according to the embodiment
20 of the present invention.

21 **[0077]** As illustrated in Fig. 10, the bias pulse voltage is applied to the scan electrode common

line YY_1 when 14 data pulse voltages are applied in succession under the conditions of Fig. 2 with T_{s-d} of 7.33 μs .

[0078] Table 2

	Pulse voltage	Pulse width (μs)
Sustain discharge pulse	155V	2
Reset 1 pulse	-190V	2
Reset 2 pulse	145V	8
Scan pulse	-80V	0.33

[0079] As shown in Fig. 11, there is no operational margin when the bias pulse voltage is 0V. The minimum data pulse voltage decreases with an increase in the bias pulse voltage. As in the case of Fig. 8, the minimum data pulse voltage is decreased to 34 V when the bias pulse voltage exceeds 50 V. On the other hand, the maximum data pulse voltage also decreases with an increase in the bias pulse voltage to narrow the operational margin. For the maximum of the operational margin, the bias pulse voltage amounts to 30 V, in which case the data pulse voltage margin is 11 V.

[0080] Hereinafter, a description will be given as to a general PDP and its driving method according to an embodiment of the present invention with reference to Figs. 12 and 13.

[0081] Fig. 12 is a general electrode connection diagram of a PDP according to an embodiment of the present invention.

[0082] The PDP according to the embodiment of the present invention is enabled to apply 14 scan pulse voltages every 10 μs , and it includes more than 240 scan electrodes. In the PDP, as illustrated

in Fig. 12, the electrodes are divided into 18 groups each of which includes 14 adjacent scan and sustain electrodes.

[0083] Namely, as shown in Fig. 12, the sustain electrodes of the same group are coupled in common to one of 18 sustain electrode common lines XX_1 to XX_{18} , and 14 scan electrodes of the same group are independently coupled to a different one of 14 scan electrode common lines YY_1 to YY_{14} .

[0084] Fig. 13 shows a driving voltage waveform for driving the PDP according to the embodiment of the present invention. In Fig. 13, one TV field consists of 92 sub-fields, each of which has a length of 180 μs .

[0085] As illustrated in Fig. 13, scan pulse voltages are applied to the scan electrode common lines YY_1 to YY_{14} between the sustain discharge voltage pulses for one TV field. The scan pulse voltage applied to the scan electrode common line YY_2 is 0.33 μs later than that applied to the scan electrode common line YY_1 . Likewise, the scan pulse voltage applied to the scan electrode common line YY_{i+1} is 0.33 μs later than that applied to the scan electrode common line YY_i . The data pulse voltage is applied to the data electrodes D_1 to D_{640} in synchronization with the scan pulse voltage.

[0086] On the other hand, reset pulse voltages are applied to the sustain electrode common lines XX_1 to XX_{18} , as shown in Fig. 13. The reset pulse voltage applied to the sustain electrode common line XX_2 is applied 10 μs later than that applied to the sustain electrode common line XX_1 . Likewise, the reset pulse voltage applied to the sustain electrode common line XX_{i+1} is applied 10 μs later than that applied to the sustain electrode common line XX_i .

[0087] To realize a 3-input AND logic operation, sustain discharge voltages are eliminated from

the sustain electrode common lines XX_1 to XX_{18} . As illustrated in Fig. 13, the sustain discharge voltage of the sustain electrode common line XX_{i+1} is eliminated $10\ \mu\text{s}$ later than that of the sustain electrode common line XX_i . The erasure of the sustain discharge voltage pulses occurs every $180\ \mu\text{s}$.

[0088] As shown in Fig. 13, the reset pulse voltage is applied to each of the sustain electrode common lines XX_1 to XX_{18} only once in one TV field. Hence, the sustain discharge occurs in succession over 92 sub-fields, because there is no rest step between the sub-fields.

[0089] In the principle of the 3-input AND logic operation, a sustain discharge does not occur for one TV field, once an address erasure is carried out to erase the sustain discharge voltage and apply the data pulse voltage in a synchronous way. The 92 sub-fields allow a display of 93 gradations.

[0090] Additionally, as shown in Fig. 13, a bias pulse is applied to the scan electrode common lines YY_1 to YY_{14} to broaden the driving margin of the data pulse voltage.

[0091] The present invention can be also realized as computer-executable instructions in computer-readable media. The computer-readable media includes all possible kinds of media in which computer-readable data is stored or included or can include any type of data that can be read by a computer or a processing unit. The computer-readable media include for example and not limited to storing media, such as magnetic storing media (*e.g.*, ROMs, floppy disks, hard disk, and the like), optical reading media (*e.g.*, CD-ROMs (compact disc-read-only memory), DVDs (digital versatile discs), re-writable versions of the optical discs, and the like), hybrid magnetic optical disks, organic disks, system memory (read-only memory, random access memory), non-volatile memory such as flash memory or any other volatile or non-volatile memory, other semiconductor media,

1 electronic media, electromagnetic media, infrared, and other communication media such as carrier
2 waves (*e.g.*, transmission via the Internet or another computer). Communication media generally
3 embodies computer-readable instructions, data structures, program modules or other data in a
4 modulated signal such as the carrier waves or other transportable mechanism including any
5 information delivery media. Computer-readable media such as communication media may include
6 wireless media such as radio frequency, infrared microwaves, and wired media such as a wired
7 network. Also, the computer-readable media can store and execute computer-readable codes that
8 are distributed in computers connected via a network. The computer readable medium also includes
9 cooperating or interconnected computer readable media that are in the processing system or are
10 distributed among multiple processing systems that may be local or remote to the processing system.
11 The present invention can include the computer-readable medium having stored thereon a data
12 structure including a plurality of fields containing data representing the techniques of the present
13 invention.

14 **[0092]** An example of a computer, but not limited to this example of the computer, that can read
15 computer readable media that includes computer-executable instructions of the present invention
16 is shown in FIG. 14. The computer 1400 includes a processor 1402 that controls the computer 1400.
17 The processor 1402 uses the system memory 1404 and a computer readable memory device 1406
18 that includes certain computer readable recording media. A system bus connects the processor 1402
19 to a network interface 1408, modem 1412 or other interface that accommodates a connection to
20 another computer or network such as the Internet. The system bus may also include an input and
21 output interface 1410 that accommodates connection to a variety of other devices.

1 **[0093]** As described above, in the method for driving a PDP according to the present invention,
2 no more than one reset pulse voltage is applied for one TV field without a reset step between the
3 respective sub-fields, thereby drastically reducing ineffective light and improving the contrast.

4 **[0094]** In the apparatus for driving a PDP according to the present invention, a plurality of scan
5 and sustain electrodes arranged in pairs are divided into j groups each including i pairs of the scan
6 and sustain electrodes, the sustain electrodes of a same group being coupled in common to j X
7 electrode common lines, and the scan electrodes of a same group being coupled independently to a
8 different one of i Y electrode common lines. Therefore, the present invention reduces the number
9 of driver IC's for the scan and sustain electrodes from $(i \times j + 1)$ to $(i + j)$, thereby lowering the cost
10 of the PDP.

11 **[0095]** Furthermore, the present invention realizes a high-brightness display because the sustain
12 discharge pulse can be applied in succession in at most one TV field.

13 **[0096]** While this invention has been described in connection with what is presently considered
14 to be the most practical and preferred embodiment, it is to be understood that the invention is not
15 limited to the disclosed embodiments, but, on the contrary, is intended to cover various
16 modifications and equivalent arrangements included within the spirit and scope of the appended
17 claims.